400G-2*VR4 OSFP Transceiver

Product Features

- 400G Breakout Mode
  2x 400GBASE-VR4
  2x 400GAUI-4
- 100G Breakout Mode
  8x 100GBASE-VR
  8x 100GAUI-1
- Form factor: OSFP800 MSA
- Optical connector: Dual MPO-12 / APC
- Power consumption: <16 W
- Operating case temperature: 0 to 70 ºC
- Management interface: CMIS 5.2

Product Applications

- 800 GbE data center interconnects
- 2x 400GbE / 8x 100GbE breakout applications

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	0	+3.6	V	
2	Storage Temperature		-40	85	°C	
3	Optical Relative Humidity	RH	5	85	%	

Recommended Operating Conditions

Table 2 Operating Environment

No	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	3.135	3.3	3.465	V	
2	Supply Voltage Noise	PSNR			66	mV	10 Hz –10

	Tolerance						MHz
3	Power Consumption	P_8			16	W	
4	Instantaneous peak current	Icc_ip_8			6400	mA	
5	Sustained peak current	Icc-sp_8			5328.0	mA	
6	Supply Current	Icc-8			5103.7	mA	
7	Case Temperature	TC	0	35	70	°C	

Note 1: Steady state current must not allow power consumption to exceed the specified maximum power for the selected power class.

Electrical Characteristics

Table 3 Electrical Characteristics

No.	Parameter	Min.	Typ.	Max.	Unit	Remarks
Module output (each lane, at TP4) [Note 1]						
1	Signaling rate per lane (range)	-100ppm	53.125	+100ppm	GBd	PAM4
2	AC Common-mode output voltage [RMS]			25	mV	
3	Differential peak-to-peak output voltage			600 845	mV	Short Mode Long Mode
4	Eye height	15			mV	
5	Vertical eye closure [VEC]			12	dB	
6	Common-mode to differential-mode return loss [RLdc]	Equation (120G-1)			dB	Note 2
7	Effective return loss [ERL]	8.5			dB	
8	Differential termination mismatch			10	%	
12	Transition time (20% to 80%)	8.5			ps	
13	DC common mode voltage (range)	-0.35		2.85	V	
Module input (each lane)						
1	Signaling rate, each lane (range)	-100ppm	53.125	+100ppm	GBd	at TP1
2	Differential pk-pk input voltage tolerance	750			mV	at TP1a

	AC common-mode RMS voltage tolerance	25			mV	at TP1a
3	Differential-mode to common-mode return loss [RLcd]	Equation (120G-3)			dB	at TP1, Note 2
4	Effective return loss [ERL]	8.5			dB	at TP1
5	Differential termination mismatch			10	%	at TP1
6	Module stressed input tolerance	See 120G.3.4.3			-	at TP1a, Note 2
7	Single-ended voltage tolerance range	-0.4		3.3	V	at TP1a
11	DC common-mode voltage tolerance (range)	-0.35		2.85	V	at TP1

Note 1: Electrical module output is squelched for loss of optical input signal. Note2: IEEE Std 802.3ck-2022 [3]

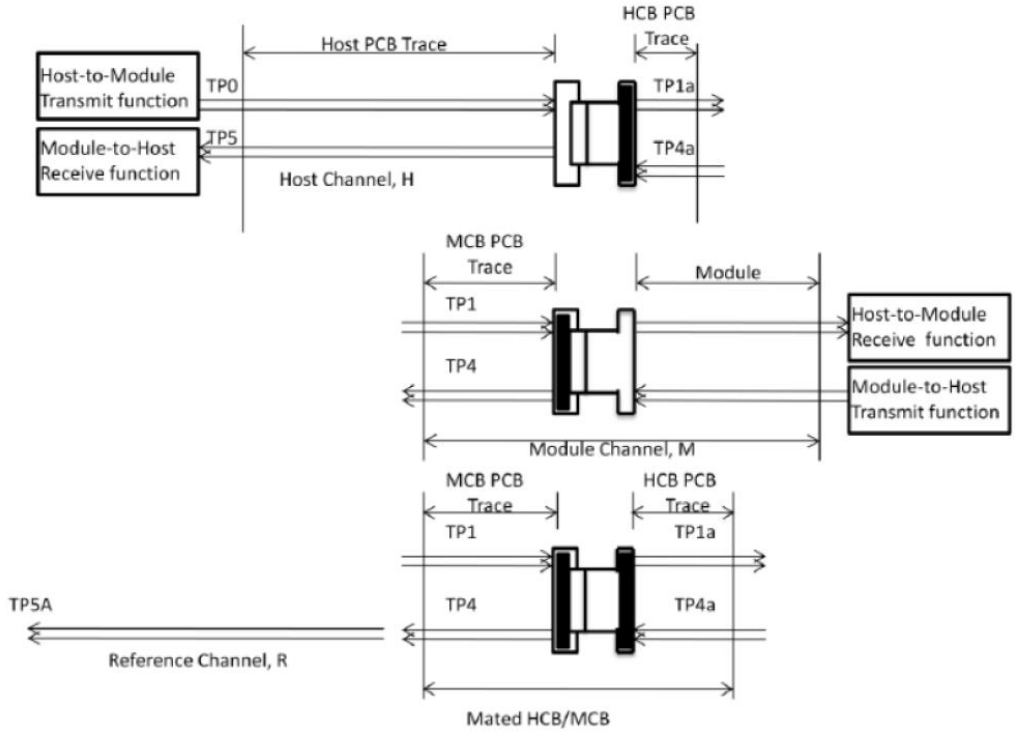


Figure1 Reference Test Points

Optical Characteristics

Table 4 Optical Characteristics (per lane)

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Channel data rate	fDC		106.25		Gb/s	
2	Signaling rate	fSG		53.125		GBd	PAM4
3	Signal speed variation from nominal	⊿fSG	-100		+100	ppm	
4	Lane wavelength (range)	λC	842		948	nm	
5	RMS Spectral width	RMS	-		0.6	nm	
6	Average launch power, each lane		-4.6		4	dBm	
7	Outer Optical Modulation Amplitude (OMAouter), each lane for max(TECQ, TDECQ)≤1.8dB for 1.8<max((TECQ, TDECQ)≤4.4dB		-2.6 -4.4		3.5	dBm	
8	Transmitter eye closure for PAM4,each lane	TECQ			4.4	dB	
9	Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			4.4	dB	
10	Average Optical Output Power of Off Transmitter, each lane	Poff			-15	dBm	
11	Extinction Ratio, each lane	ER	2.5			dB	
12	RIN12OMA				-131	dB/Hz	
13	Optical return loss tolerance				12	dB	
15	Average receive power, each lane		–6.4		4.0	dBm	
14	Damage Threshold		5			dBm	Note 1
16	Receive power (OMAouter), each lane				3.5	dBm	
17	Receiver reflectance				-12	dB	

18	Receiver sensitivity (OMAouter), each lane for TECQ≤1.8dB for 1.8 <TECQ≤4.4dB	SOMA			-4.6 -6.4	dBm	
19	Stressed receiver sensitivity (OMAouter), each lane	SRS			-2	dBm	Note 2
Conditions of stressed receiver sensitivity test [Note 3]							
20	Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	4.4			dB	
21	OMAouter of each aggressor lane		3.5			dBm	

Note 1: The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.

Note 2: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note 3: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

High-Speed Signals

The high-speed signals consist of 8 transmit and 8 receive differential pairs identified as TX[8:1]p / TX[8:1]n and RX[8:1]p / RX[8:1]n. These signals can be operated in port configurations of either octa 2-lanes or quad 2-lanes or 8 individual 2-lanes depending on the capability of the host ASIC.

800GAUI-8 or 2x400GAUI-4 or 8x100GAUI-1 mode provides 8 differential lanes using 112G-PAM4 signaling operating at 53.125 Gbaud. This results in 8 lanes of 100Gb/s for a total of 800Gb/s. This mode allows connection to PMD configurations of 1x800G or 2x400G or 8x100G.

The high-speed signals follow the electrical specifications is shown in Table.

Low-Speed Signals

There are 4 low-speed signals consisting of SCL, SDA, LPWn/PRSn and INT/RSTn. These signals are used for configuration and control of the module by the host. SCL and SDA use 3.3V LVCMOS levels and are bidirectional signals.

LPWn/PRSn and INT/RSTn have additional circuitry on the host and module to enable multi-level bidirectional signaling.

SCL and SDA (2-Wire Management Interface)

SCL and SDA are a 2-wire serial interface between the host and module using the I2C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open-drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

The host shall default to using 100 kbit/s standard-mode I2C when first accessing an unidentified module for backward compatibility. Once the module has been brought out of reset, the host can read the module' s 2-wire interface speed register to determine the maximum supported speed the module allows. For an OSFP, the host may then use I2C FPHOS-mode, as indicated by the module. It is optional for the host to change the speed of the 2-wire interface but remaining at a low speed could lead to slow management transactions for modules that require frequent accesses.

SCL and SDA signals follow the electrical specifications of FPHOS-mode are shown in Table 6.

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This OSFP800 specification is based on SFF-8636 [7] but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636 [7]. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the OSFP memory map rather than the QSFP memory map.

The OSFP800 Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. OSFP800 two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. The timing requirements on the two- wire interface are listed

in Table 6 and Figure 3.

Table 5 Management Interface Timing

Parameter	Symbol	(400 kHz)		Unit	Conditions
		Min	Max		
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		μs	
Clock Pulse Width High	tHIGH	0.6		μs	
Time bus free before new transmission can start	tBUF	20		μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		μs	
Data In Setup Time	tSU.DAT	0.1		μs	
Input Rise Time	tR		300	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		μs	
STOP Hold Time	tHD.STO	0.6		us	
Aborted sequence bus release	Deselect _Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP112 module releasing SCL and SDA
ModSelL Setup Time1	tSU.ModSelL	2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time1	tHD.ModSelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.

Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		500	us	Time the QSFP112 module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory.	tNACK		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		cycles	Module Case Temperature= 70 °C

Note 1: The management registers can be read to determine alternate support for ModSelL set up and hold times. See CMIS 8.4.5, Durations Advertising or SFF-8636 6.2.9, Free Side Device Properties (Page 00h, Bytes 107-115).

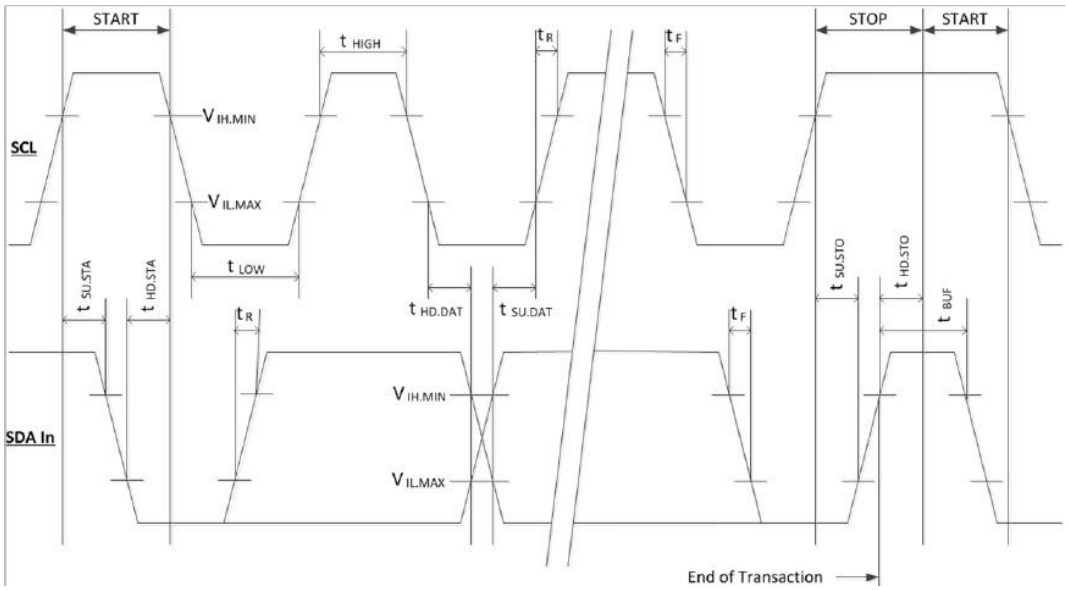


Figure 2 2-Wire Interface Timing Diagram

INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 6 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is

translated to an active- low signal on the module. Interrupt is an active-high signal on the module which gets translated to an active- high signal on the host.

The INT/RSTn signal operates in 3 voltage zones to indicate the state of Reset for the module and Interrupt for the host. Figure 5 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_INT signal and the module uses a voltage reference at 1.25V to determine the state of the M_RSTn signal.

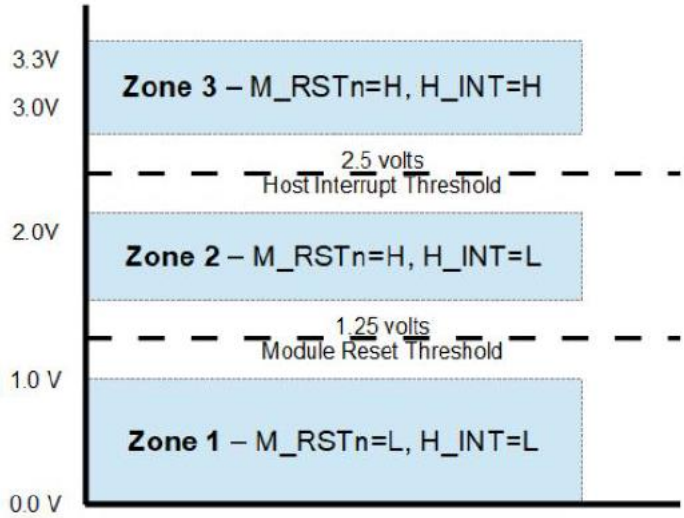


Figure 3 INT/RSTn voltage zones

Zone 1 - Reset operation - Zone 1 is the state when the module is in reset and interrupt deasserted (M_RSTn=Low, H_INT=Low). The min/max voltages for Zone 1 are defined by parameters V_INT/RSTn_1 and V_INT/RSTn_2 in Table.

Zone 2 - Normal operation - Zone 2 is the normal operating state with reset deasserted (M_RSTn=High) and interrupt deasserted (H_INT=Low). The min/max voltages for Zone 2 are defined by parameter V_INT/RSTn_3 in Table.

Zone 3 - Interrupt operation - Zone 3 is the state for the module to assert interrupt and the module must also be out of reset (M_RSTn=High, H_INT=High). The min/max voltages for Zone 3 are defined by parameter V_INT/RSTn_4 in Table.

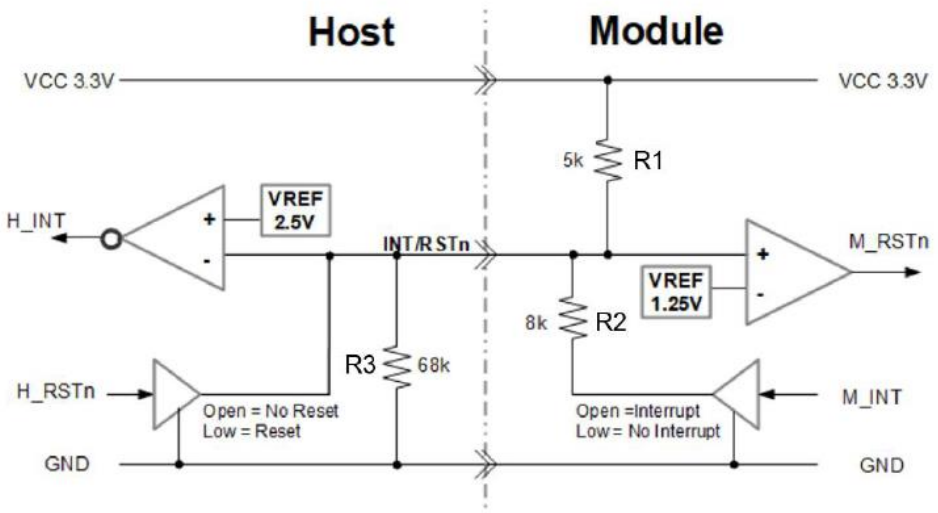


Figure4 INT/RSTn circuit

INT/RSTn circuit parameters

Table 6 INT/RSTn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H Vref INT	2.500	2.475	2.525	Volts	Precision voltage reference for H INT
M Vref RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M RSTn
Rl	68k	66k	70k	Ohms	Recommend 68.lk ohms 196resistor
R2	Sk	4.9k	5.lk	Ohms	Recommend 4.99k ohms 196resistor
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V INT/RSTn 1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V INT/RSTn 2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M INT=High

The functionality and implementation has not changed but the description has been updated to use the non-inverted signal (H_INT) instead of the inverted signal (H_INTn). This makes the polarity of the interrupt signal the same between the module (M_INT) and host (H_INT) for better clarity. This is purely a description change with no change to functionality. Host implementations with an inverted interrupt signal are fully OSFP MSA specification [4] compliant.

LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 8 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signal on the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

The LPWn/PRSn signal operates in 3 voltage zones to indicate the state of Low Power mode for the module and Module Present for the host. Figure 7 shows these 3 zones. The host uses a voltage reference at 2.5 volts to determine the state of the H_PRSn signal and the module uses a voltage reference at 1.25V to determine the state of the M_LPWn signal.

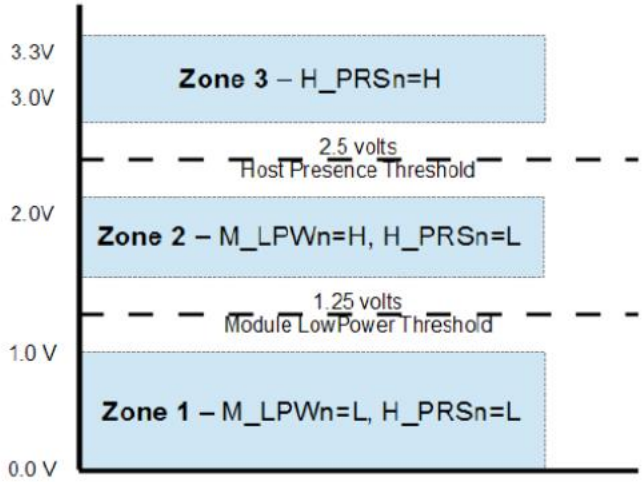


Figure 5 LPWn/PRSn voltage zones

Zone 1 - Low Power mode - Zone 1 is the low power state and module is present (M_LPWn=Low, H_PRSn=Low). The min/max voltages for Zone 1 are defined by parameters V_LPWn/PRSn_1 in Table 8.

Zone 2 - High Power mode - Zone 2 is the high power state and module is present (M_LPWn=High, H_PRSn=Low). The min/max voltages for Zone 2 are defined by parameters V_LPWn/PRSn_2 in Table 8.

Zone 3 - Module Not Present - Zone 3 is the state for when the module is not present (H_PRSn=High). The min/max voltages for Zone 3 are defined by parameters V_LPWn/PRSn_3 in Table 8.

Module Removal - If the module is being unplugged and LPWn/PRSn loses contact, the pull-down resistor on the module asserts Low Power mode on the module (M_LPWn=Low). The module is required to transition to low power (Power Class 1) and disable transmitters within the time specified by T_hplp in Table13. This maximum transition time is to ensure the module is in Low Power mode before the power contacts lose connection to avoid potential damage from arcing.

The LPWn/PRSn signal is driven High or Open by the host for Low Power mode control. If logic is used to generate the High level then 3.3V LVCMOS is preferred.

For very low cost modules, such as DAC, the voltage comparator on the module may be omitted and the LPWn/PRSn pin in that case is tied to GND in the module. This type of module may only be used for low power mode (Power Class 1).

The module transmitters must be disabled when in Low Power mode. This ensures Power Class 1 and also provides a fast hardware shut down mechanism for applications such as redundancy switch-over. In addition, software controlled transmitter disable is provided by the TX Disable register via the I2C interface.

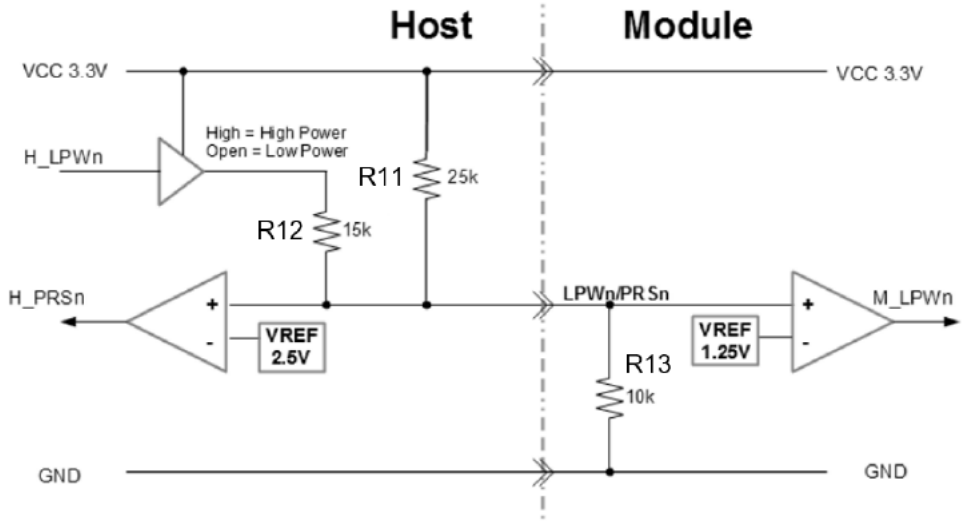


Figure 6 LPWn/PRSn circuit

Table 7 LPWn/PRSn circuit parameters

Parameter	Nominal	Min	Max	Units	Note
HostVCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H Vref PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
Rll	25k	24.Sk	25.Sk	Ohms	Recommend 24.9k ohms 1% resistor
R12	15k	14.7k	15.3k	Ohms	Recommend lSkohms 1% resistor
R13	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V LPWn/PRSn 1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, HLPWn=Low
V LPWn/PRSn 2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage fo『Module installed, HLPWn=High
V LPWn/PRSn 3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

Soft Control and Status Functions

Table 9 lists the required timing performance for software control and status functions.

Table 8 Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions

MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on[1], hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		μs	Minimum pulse time on the Low RSTn signal to initiate a module reset.
INT/PRSn Mode Change	t_ INT/PRSn		100	ms	Time to change between INT and PRSn modes of the signal INT/PRSn.
LPWn/RSTn mode change time	t_ LPWn/RSTn		100	ms	Time to change between LPWn and RSTn modes of LPWn/RSTn.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:INT=Low.
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read[2] operation of associated flag until Vout:INT=High. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
TX Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.
TX Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 1 until optical output rises above 90% of nominal4.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)5 until associated IntL assertion is inhibited.

Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)5 until associated Low INT operation resumes.

Note 1: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 2.

Note 2: Measured from the rising edge of SDA in the stop bit of the read transaction. Note 3: Rx LOS condition is defined at the optical input by the relevant standard.

Note 4: Tx Squelch Deassert time is longer than SFF-8679 [8].

Note 5: Measured from the rising edge of SDA in the stop bit of the write transaction.

Squelch and Disable Assert/De-assert and Enable/Disable Timing

Table 9 I/O Timing for Squelch & Disable

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached,
Tx Squelch De-assert Time	toff_Txsq	2	s	Tx squelch deassert is system and implementation dependent.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence1 until optical output falls below 10% of nominal.
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)[1] until optical output falls below 10% of nominal and see notes 2 and 3.
Tx Disable De-assert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal and see note 2.
Tx Disable De-assert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)[1] until optical output rises above 90% of nominal, see note 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)[1] until Rx output falls below 10% of nominal
Rx Output Disable De-assert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)[1] until Rx output rises above 90% of nominal.

Squelch Disable Assert Time	ton_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)[1] until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis	Not applicable (Tx/Rx Auto Squelch Disable not supported)	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)[1] until squelch functionality is enabled.

Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction. Note 2. CMIS 4.0 and beyond the listed values are superseded by the advertised DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times in P01h.168.

Note 3. Listed values place a limit on the DataPathTxTurnOff_MaxDuration and DataPathTxTurnOn_MaxDuration times (P01h.168) that can be advertised by such modules (for CMIS 4.0 and beyond).

POWER

The power supply has four designated Vcc pins in the connector. Power is applied concurrently to these pins.

A host board together with the OSFP800 module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

All power supply requirements in Table 2 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

OSFP800 modules are categorized into several power classes as listed in Table 11. The power class of TRJ2JVPPNFDMF is class 8.

Table 10 Maximum Power Classes

Power Class	Max Power (W)	CMIS Register
1	1.5	Direct readout of Page 00h Byte 200[000xxxxx]
2	3.5	Direct readout of Page 00h Byte 200[001xxxxx]
3	7.0	Direct readout of Page 00h Byte 200[010xxxxx]
4	8.0	Direct readout of Page 00h Byte 200[011xxxxx]
5	10	Direct readout of Page 00h Byte 200[100xxxxx]
6	12	Direct readout of Page 00h Byte 200[101xxxxx]
7	14	Direct readout of Page 00h Byte 200[110xxxxx]
8 [1]	>14	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8 the host must read CMIS Page 00h Byte 201 to determine module power dissipation. Please see CMIS Byte 201 register definition for more information.		

Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 7.

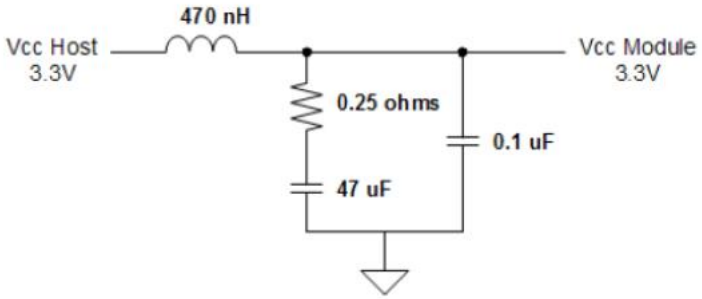


Figure 7 Recommended Host Board Power Supply Filtering

OSFP Module Power Up Behavior

The OSFP module powers up when system power is enabled or on module insertion or on VCC power enable to the module. Once powered, the module either waits in Low Power mode or enters High Power mode based on the state of the Reset signal, Low Power signal and ForceLowPwr bit of the module. The ForceLowPwr bit default is pre-programmed in the module by the manufacturer and typically would be set to 0. The host can change the ForceLowPwr bit after power up but it returns to its pre-programmed default when the module is placed in reset or power cycled. The Reset and Low Power signals are described in

sections 4.2 and 4.3. The ForceLowPwr bit is defined in the OSFP Management Interface Specification.

The table below shows the module power up state based on Low Power and ForceLowPwr. If LPWn=0 then the module goes to low power mode and transmitters disabled. If ForceLowPwr=0 and LPWn=1 then the module immediately enables transmitters. If ForceLowPwr=1 and LPWn=1 then the module waits in Low Power mode until the host clears the ForceLowPwr bit for the module to enable transmitters.

Table 11 Power up behavior

Module State	ForcelowPwr =O	ForcelowPwr =1
Low Power asserted (LPWn = 0)	Low Power Mode (transmitters Disabled)	Low Power Mode (transmitters Disabled)
Low Power de-asserted (LPWn = I}	Operational (transmitters Enabled*)	Low Power Mode (transmitters Disabled)

* The host may use the management interface to alter this default behavior

OSFP Module Reset Behavior

Reset is a hardware signal from the INT/RSTn pin as defined in section 4.2. Asserting Reset overrides all other hardware and software controls and forces the module into the Reset state. This includes forcing Low Power mode and disabling transmitters.

Module Power Supply Specification

+3.3V power is delivered to the module via 4 power pins (VCC). These 4 power pins are connected together on the module and also together on the host. Each power pin allows up to 2.5 Amps for a total of 10.0 Amps. This enables a maximum power in excess of 30 Watts.

The specification of the module power is in accordance with methods defined by SFF-8679 Rev 1.7 section5.5[8]. There are 8 power classes defined as shown

in Table 11. All modules in reset or the default low power mode must comply with Power Class 1. High power mode enables the module to draw power up to its advertised power class, and may be conditionally enabled by the host. The host may read the module power class register to know the power class of the module before or after enabling high power mode. The module does not exceed the power class it identifies for itself.

Transition between low and high power mode is controlled by the M_RSTn (reset) signal, M_LPWn (low power mode) signal and ForceLowPwr bit. The module remains in or transition to low power mode when M_LPWn or M_RSTn are asserted or the ForceLowPwr bit is set. While in low power mode, active modules also disables transmitters. The module may transition to high power mode once M_RSTn and M_LPWn are deasserted and the ForceLowPwr bit is cleared.

The specifications of Table 11 and Table 13 are for the combined power of all 4 power pins. The measurement location for these specifications is at the OSFP connector VCC pins on the host board.

Table 12 OSFP power specification

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.201	3.300	3.465	V
Voltage drop across mated connector (Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV
Total current for Vcc pins (Note 1)	Icc_module			10.0	A
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (Note 2)	I_didt			100	mA/µs
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs

PIN ASSIGNMENT

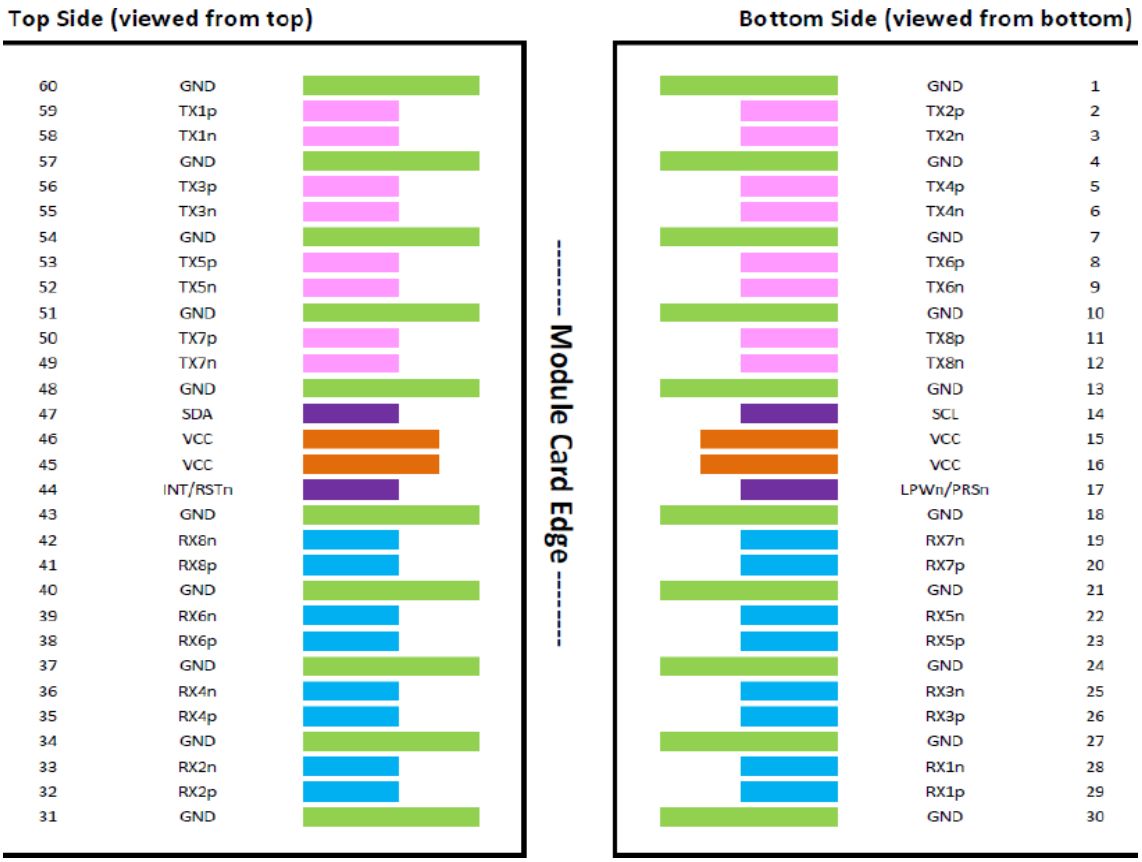


Figure8 Module Pads

The electrical interface of an OSFP module consists of a 60 contacts edge connector as illustrated by the diagram in Figure 10. It provides 16 contacts for 8 differential pairs of high-speed transmit signals, 16 contacts for 8 differential pairs of high-speed receive signals, 4 contacts for low-speed control signals, 4 contacts for power and 20 contacts for ground.

The edge connector pads have 3 different pad lengths to enable sequencing of the contacts to protect the module against electrostatic discharge (ESD) and provide reliable power up/power down sequencing for the module during insertion and removal. The ground pads are the longest for first contact, the power pads are the second longest for second contact and the signal pads are the third longest for final contact during insertion.

The chassis ground (case common) of the OSFP module is isolated from the module' s circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module. When an OSFP module is not installed, the signals to the connector within the unused cage should be disabled to minimize electromagnetic interference (EMI) emissions.

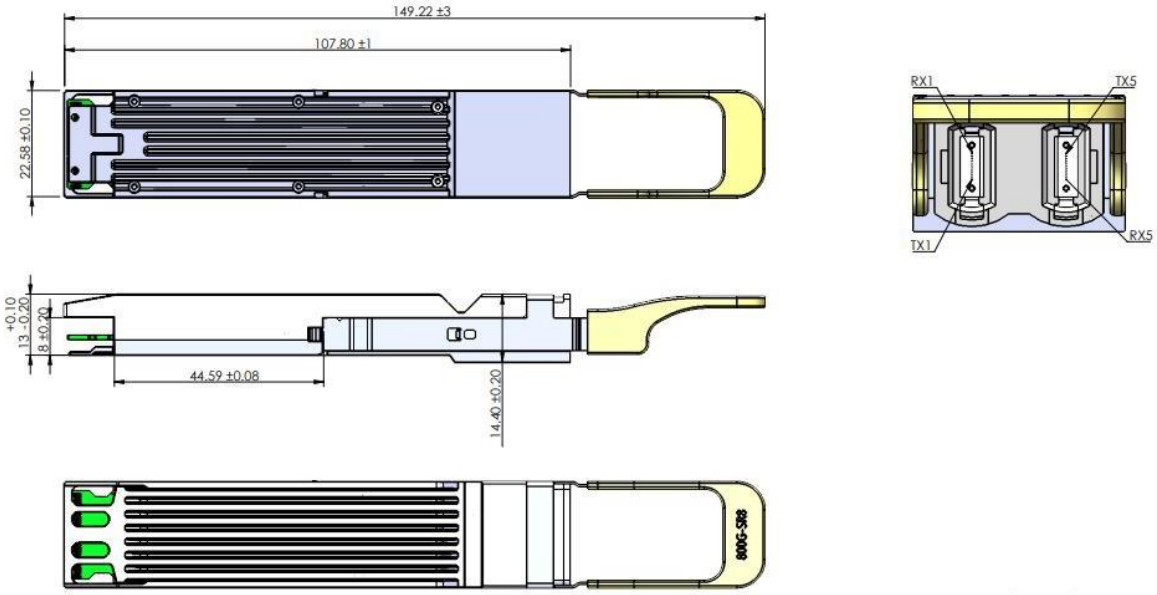
Table 13 Pin List

PIN	Logic	Symbol	Definition	PIN	Logic	Symbol	Definition
1		GND	Ground	31		GND	Ground
2	CML-I	Tx2p	Transmitter Data Non-Inverted	32	CML-O	Rx2p	Receiver Data Non-Inverted
3	CML-I	Tx2n	Transmitter Data Inverted	33	CML-O	Rx2n	Receiver Data Inverted
4		GND	Ground	34		GND	Ground
5	CML-I	Tx4p	Transmitter Data Non-Inverted	35	CML-O	Rx4p	Receiver Data Non-Inverted
6	CML-I	Tx4n	Transmitter Data Inverted	36	CML-O	Rx4n	Receiver Data Inverted
7		GND	Ground	37		GND	Ground
8	CML-I	Tx6p	Transmitter Data Non-Inverted	38	CML-O	Rx6p	Receiver Data Non-Inverted
9	CML-I	Tx6n	Transmitter Data Inverted	39	CML-O	Rx6n	Receiver Data Inverted
10		GND	Ground	40		GND	Ground
11	CML-I	Tx8p	Transmitter Data Non-Inverted	41	CML-O	Rx8p	Receiver Data Non-Inverted
12	CML-I	Tx8n	Transmitter Data Inverted	42	CML-O	Rx8n	Receiver Data Inverted
13		GND	Ground	43		GND	Ground
14	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset
15		Vcc	+3.3 V Power Supply	45		Vcc	+3.3 V Power Supply
16		Vcc	+3.3 V Power Supply	46		Vcc	+3.3 V Power Supply
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	47	LVCMOS-I/O	SDA	2-wire Serial interface data
18		GND	Ground	48		GND	Ground
19	CML-O	Rx7n	Receiver Data Inverted	49	CML-I	Tx7n	Transmitter Data Inverted

20	CML-O	Rx7p	Receiver Data Non-Inverted	50	CML-I	Tx7p	Transmitter Data Non-Inverted
21		GND	Ground	51		GND	Ground
22	CML-O	Rx5n	Receiver Data Inverted	52	CML-I	Tx5n	Transmitter Data Inverted
23	CML-O	Rx5p	Receiver Data Non-Inverted	53	CML-I	Tx5p	Transmitter Data Non-Inverted
24		GND	Ground	54		GND	Ground
25	CML-O	Rx3n	Receiver Data Inverted	55	CML-I	Tx3n	Transmitter Data Inverted
26	CML-O	Rx3p	Receiver Data Non-Inverted	56	CML-I	Tx3p	Transmitter Data Non-Inverted
27		GND	Ground	57		GND	Ground
28	CML-O	Rx1n	Receiver Data Inverted	58	CML-I	Tx1n	Transmitter Data Inverted
29	CML-O	Rx1p	Receiver Data Non-Inverted	59	CML-I	Tx1p	Transmitter Data Non-Inverted
30		GND	Ground	60		GND	Ground

MECHANICAL DIMENSIONS

[Unit: mm]



Pull tab color: beige

Figure 9 Mechanical Dimensions and